FIGURE 1

FIG. 2

512 KB
D-Cache
8-Ways

PRIOR ART

64 Byte L2 Line

128 bits (0)
128 bits (1)
128 bits (2)
128 bits (3)

2048 X 128 = 262144 bits = 32 KBytes

2048 words
512 L2 Lines

128 bits

A

256 KB D-Cache

B

2048 words
512 L2 Lines

128 bits

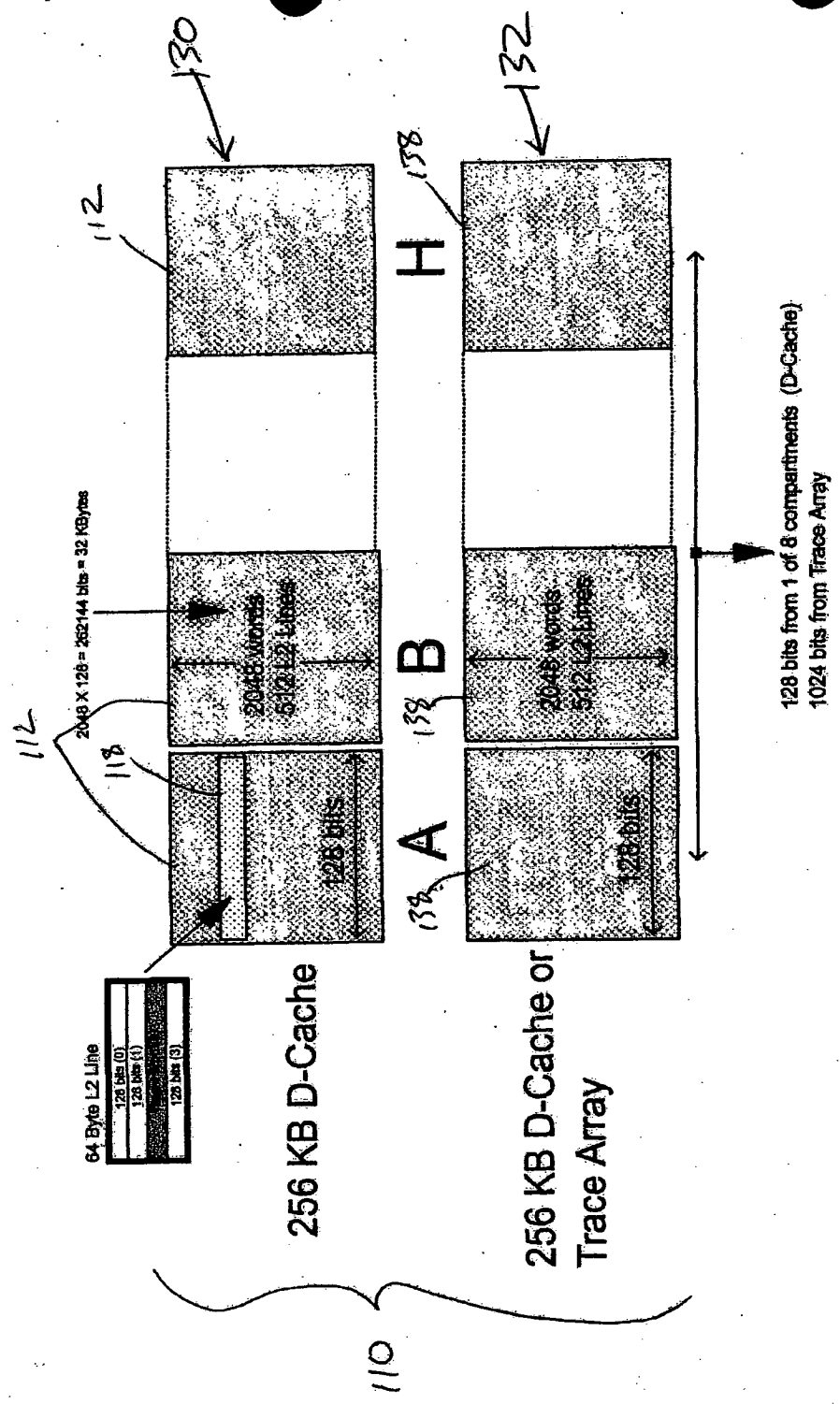256 KB D-Cache or Trace Array

H

128 bits from 1 of 8 compartments (D-Cache)
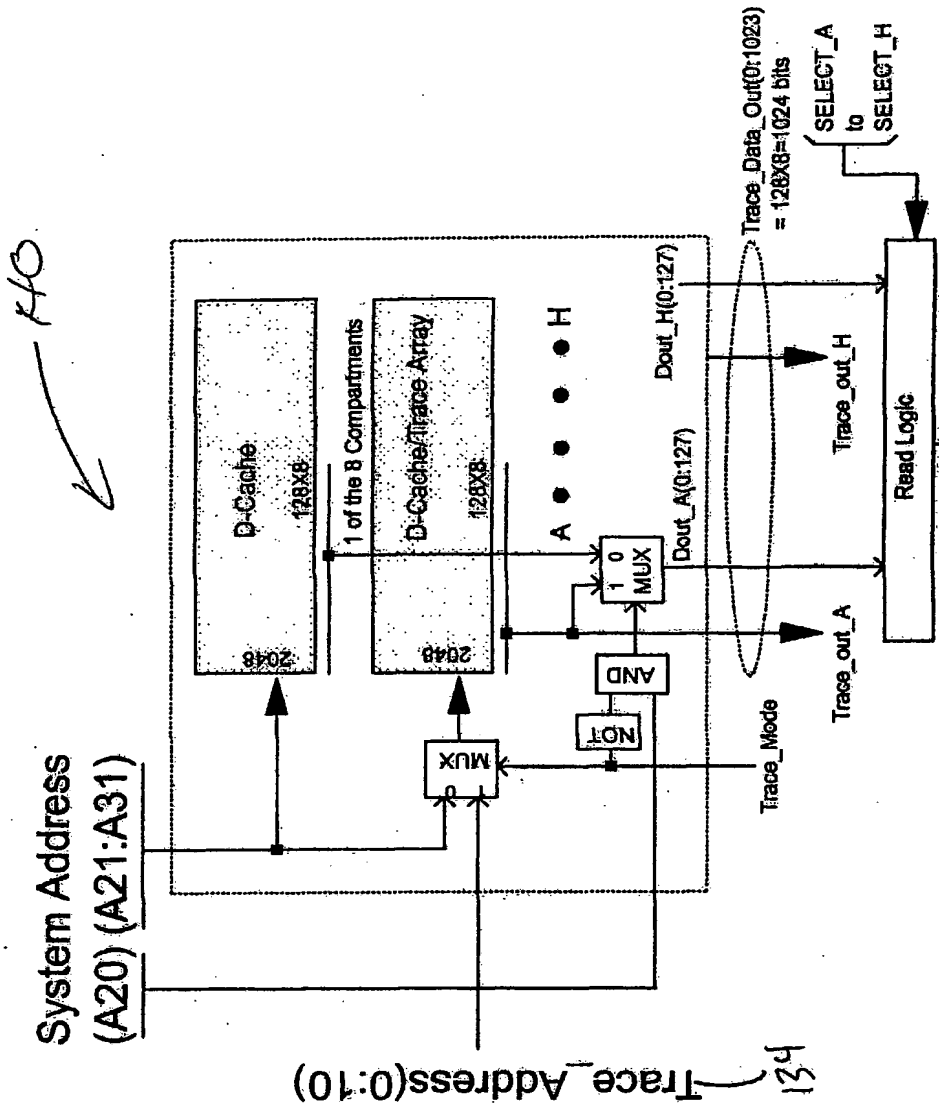1024 bits from Trace Array

Normal Mode: 512 KB D-Cache
Trace Mode: 256 KB D-Cache and
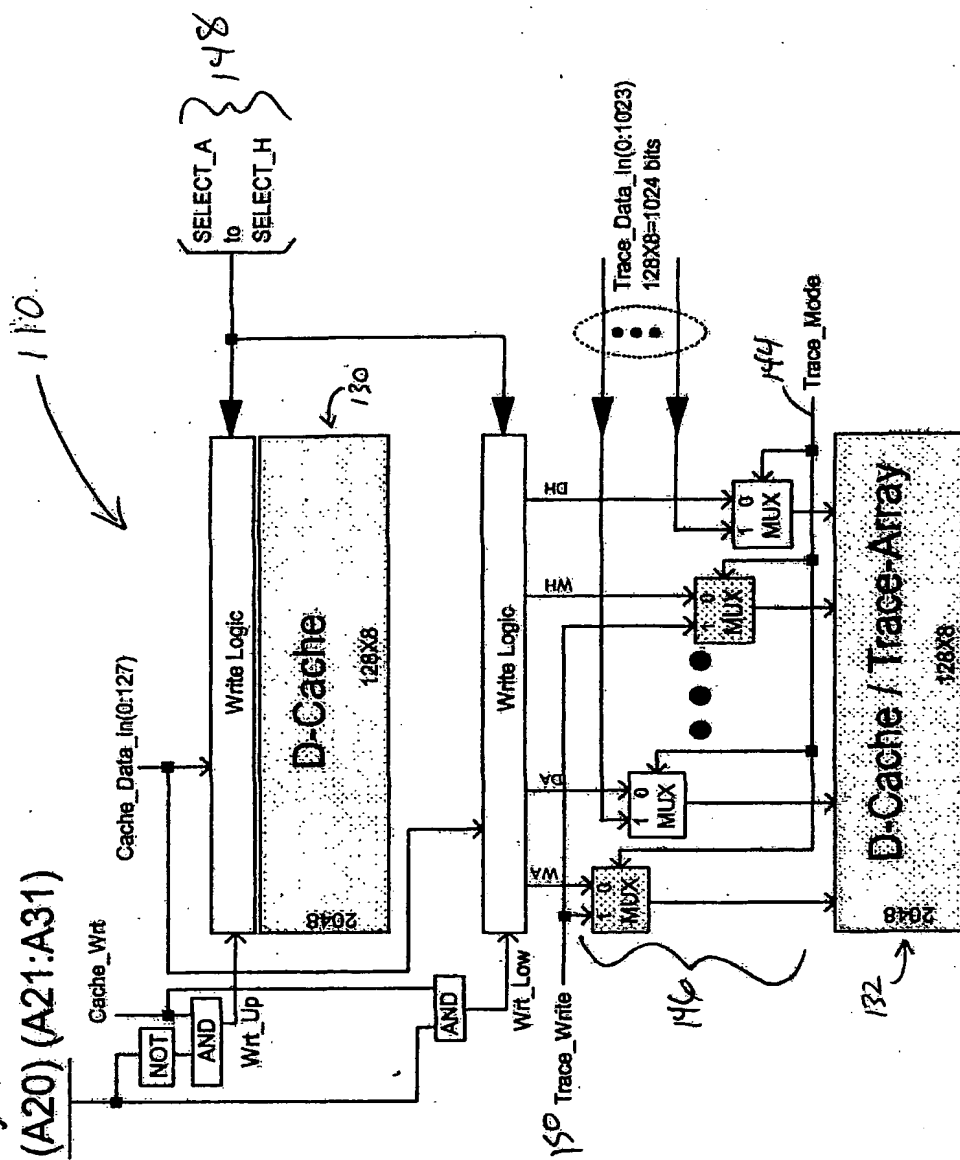256 KB Trace Array

FIG. 3

Dual function D-Cache
(Read Mode)
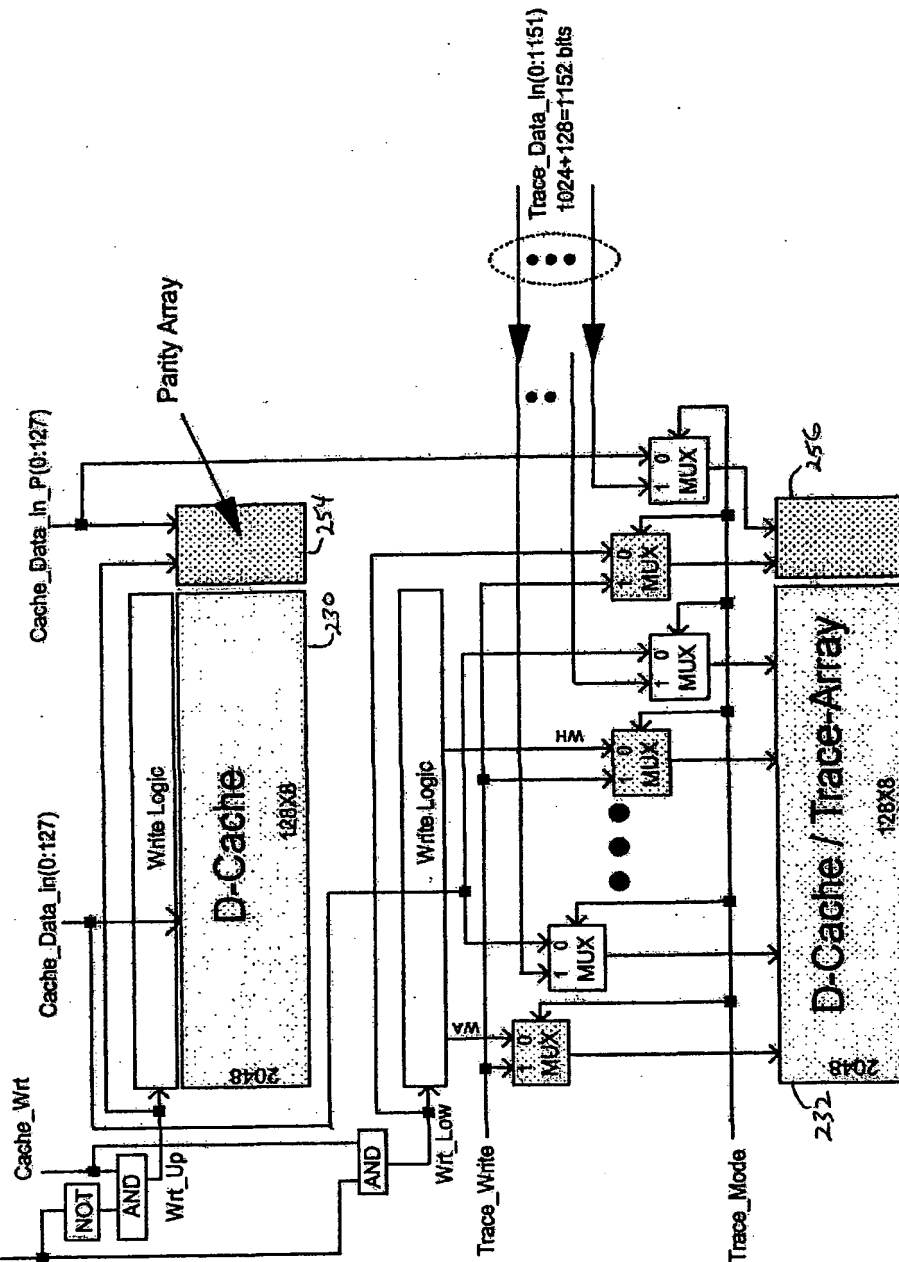
FIG. 4

System Address
(A20) (A21:A31)

110

SELECT_A
to
SELECT_H   148

Cache_Data_In(0:127)

Write Logic

D-Cache
128X8
2048

130

Cache_Wrt

NOT

AND

Wrt_Up

Write Logic

Wrt_Low

AND

150 Trace_Write

Trace_Data_In(0:1023)
128X8=1024 bits

144 Trace_Mode

DH

1 0
MUX

WH

0
MUX

DA

1 0
MUX

WA

MUX

146

D-Cache / Trace-Array
128X8
2048

132

Dual function D-Cache (Write Mode), Address
Control not shown (Same as Read Mode)

FIG. 5

Dual function D-Cache (Write Mode).
Parity Array as Trace.

FIG. 6
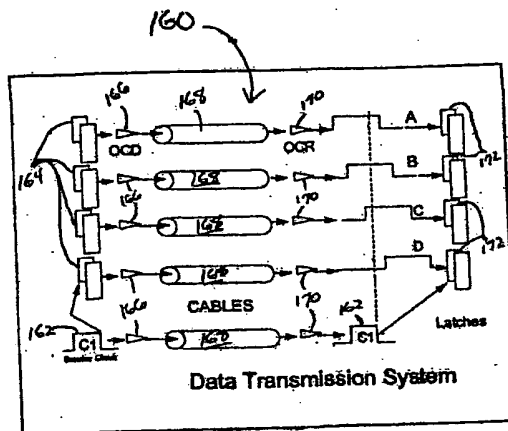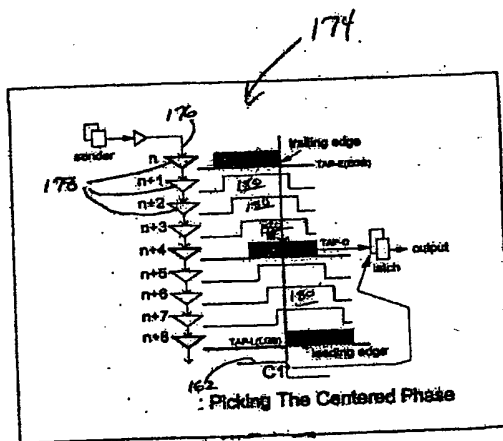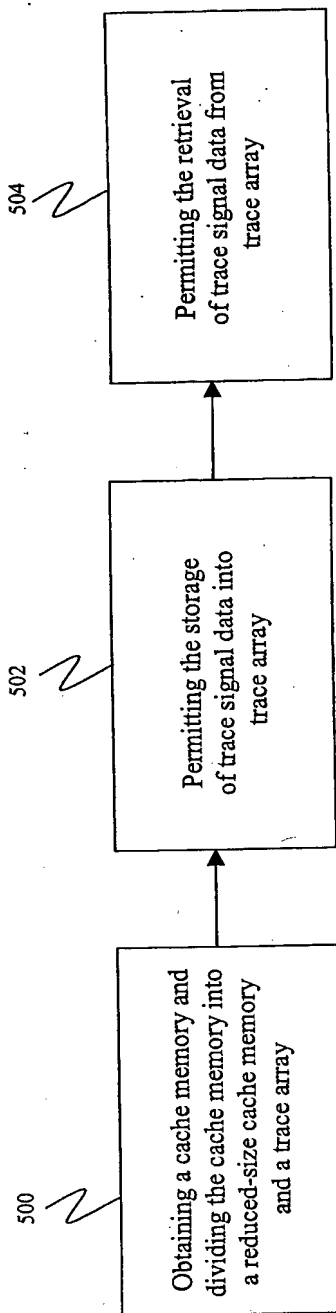
FIGURE 7

FIGURE 8

FIGURE 9

500	Obtaining a cache memory and dividing the cache memory into a reduced-size cache memory and a trace array	→

502	Permitting the storage of trace signal data into trace array	→

504	Permitting the retrieval of trace signal data from trace array

FIGURE 10